

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 01997-254002	Application No. 09/377,372
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))		Applicant Arvind Mithal et al.	
		Filing Date August 19, 1999	Group Art Unit 2731

<b>U.S. Patent Documents</b>							
Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						

<b>Foreign Patent Documents or Published Foreign Patent Applications</b>							
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
	AB	*EP 0329233	10/02/89	European Patent Office			
	AC	*EP 0 82902120 A2	09/12/97	European Patent Office			
	AD						

<b>Other Documents (include Author, Title, Date, and Place of Publication)</b>		
Examiner Initial	Desig. ID	Document
	AE	Arvind et al., "Using Term Rewriting Systems to Design and Verify Processors", IEEE Micro Special Issue, May/June 1999
	AF	Babb et al., "Parallelizing Applications into Silicon", MIT Laboratory of Computer Science, April 1999
	AG	Cook et al., "Formal verification of explicitly parallel microprocessors", March 5, 1999
	AH	Gupta et al., "Hardware-software Co-synthesis for Digital Systems", Computer Science Laboratory, Stanford University, 1993
	AI	Liao et al., "An Efficient Implementation of Reactivity for Modeling Hardware in the Scenic Design Environment", University of California at Irvine, 1997
	AJ	Matthews et al., "Microprocessor Specification in Hawk", 1998
	AK	Poyneer et al., "A TRS Model for a Modern Microprocessor", MIT Computation Structures Group Memo 408, June 25, 1998
	AL	Shen et al., "Design and Verification of Speculative Processors", MIT Computations Structures Group Memo 400 (B), 1998
	AM	Shen et al., "Modeling and Verification of ISA Implementations", MIT Computations Structures Group Memo 400 (A), 1998
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	AO	Subrahmanyam et al., "Automated Synthesis of Mixed-Mode (Asynchronous and Synchronous) Systems AT&T Technical Journal (January 1991)
	AP	Windley, P., "Verifying Pipelined Microprocessors", Brigham Young University, 1995
	AQ	Windley, P., "Specifying Instruction-Set Architectures in HOL: A Primer", Brigham Young University, 1994

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>Notice of References Cited</b>	Application/Control No. 09/377,372	Applicant(s)/Patent Under Reexamination MITHAL ET AL.	
	Examiner Brian D Nguyen	Art Unit 2661	Page 1 of 1

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	B	US-5,905,664	05-1999	Ko et al.	708/491
	C	US-5,541,850	07-1996	Vander Zanden et al.	716/18
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	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

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	N					
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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